A 2D MODELLING OF THERMAL HEAT SINK FOR IMPATT AT HIGH POWER MMW FREQUENCY

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ABSTRACT

A very useful method of formulating the Total Thermal Resistance of ordinary mesa structure of DDR IMPATT diode oscillators are presented in this paper. The main aim of this paper is to provide a 2D model for Si and SiC based IMPATT having different heat sinks (Type IIA diamond and copper) at high power MMW frequency and study the characteristics of Total thermal resistance versus diode diameter for both the devices. Calculations of Total thermal resistances associated with different DDR IMPATT diodes with different base materials operating at 94 GHz (W-Band) are included in this paper using the author's developed formulation for both type-IIA diamond and copper semi-infinite heat sinks separately. Heat Sinks are designed using both type-IIA diamond and copper for all those diodes to operate near 500 K (which is well below the burn-out temperatures of all those base materials) for CW steady state operation. Results are provided in the form of necessary graphs and tables.

KEYWORDS

IMPATT Diode, Junction Temperature, Lumped Analytical Model, Thermal Resistance, Heat sink

1. INTRODUCTION

Avalanche Transit Time (ATT) Diodes which include IMPATTs, TRAPATTs, and BARITTs and so on are potential solid-state sources for Microwave power. In the past decade the advances in IMPATT device technology has made it possible to use this device in various communication systems operating in millimeter wave and sub-millimeter wave bands of frequency ranges which provides advantages such as increased resolution and use of low voltage power supplies. The availability of several atmospheric window frequencies in the mm-wave frequency range (30-300 GHz) has further increased the usefulness of IMPATT diodes which can now produce appreciable amounts of millimeter wave power at very high frequencies of operation. Conventional Si and GaAs based IMPATT diodes were found to be reliable but they are limited by power and operating frequencies due to the limitation imposed by their inherent material parameters. Wide Band Gap (WBG) semiconductor such as Silicon Carbide (SiC) has received remarkable attention

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during the last decade as a promising device material for high-temperature, high-frequency and high- power device applications due to its high thermal conductivity, high saturation velocity of charge carriers and high critical field for breakdown. For this reason the author has chosen 4H-SiC as the base material. SiC crystallizes in numerous polytypes. The three most common polytypes are the cubic phase, 3C and the hexagonal phases, 4H, and 6H-SiC. The cubic structure, referred to as β-SiC, is expected to have the highest saturation drift velocity. However, the energy band gap of the 3C phase is significantly smaller than either the 4H or 6H phases, implying a lower breakdown voltage. In addition to this, β-SiC is difficult to grow in a mono-crystalline form due to its meta-stability resulting in a solid-state transformation into an alpha (α)-structure. Due to difficulty in the growth of β-SiC, most of the efforts for producing bulk monocrystalline growth have concentrated on the more easily prepared α-polytypes, referred to as 4H-SiC and 6H-SiC. Thus due to the availability and quality of reproducible single-crystal wafers in these polytypes, 4H- and 6H-SiC-based electronic devices presently exhibit the most promise. The energy band gap of >3.0 eV in hexagonal (4H and 6H) SiC enables the devices based on such materials, to support peak internal electric field (Ec) about ten times higher than Si and GaAs. Higher Ec increases the breakdown voltage, an essential criterion for generation of high output power in a device. Higher electric field (Ec) also permits incorporation of higher doping level in the depletion layer of the device, which in turn, reduces the width of the active region. Thus the device layers can be made very thin. The transit times of carriers become very small in a thin layered semiconductor if the carrier drift velocities are high. The intrinsic material parameters of hexagonal SiC are thus favorable for the realization of high power devices. It is well known that the efficiency of the IMPATT diode is relatively low [Practically 5-15% for CW operation], a large fraction of the dc power is dissipated as heat in the high-field region. For this reason the temperature of the junction rises above ambient, and in many cases output power of oscillator is limited by the rate at which heat can be extracted from the device. As junction temperature increases, the reverse saturation current rises exponentially and eventually leads to *thermal runway phenomenon* resulting the burning out of the device. Since in contrast to the avalanche current, the reverse saturation current does not require a large voltage to sustain it, the voltage begins to decrease when the junction gets hot enough for the reverse current to constitute a significant fraction of the total current. A thermally induced DC negative resistance is produced, causing the current to concentrate in the hottest part of the diode. As well as leading to the eventual burn-out of the junction, the increased saturation current at elevated temperatures produces degradation in the oscillator performance at power levels below the burn-out value. The increased reverse saturation current produces a faster build-up of the avalanche current and degrades the negative resistance of the device. Thus, in general, the oscillator efficiency will begin to decrease at power levels just below the burn-out power. As the band-gap of the semiconductor becomes larger the reverse saturation current associated with it becomes smaller and consequently the burn-out temperature of the junction rises. Properly designed diode and heat-sink are required for generating appreciable RF power from the CW Si-IMPATT oscillators without device burn-out during steady state operation.

Due to very small DC to RF conversion efficiency of the CW IMPATT devices a large amount of the DC power actually dissipated in the device during steady state operation of the oscillator. That actually increases its internal temperature i.e. junction temperature well above the ambient temperature. If the device's junction temperature becomes too high, the device may suffer permanent damage or burn-out. This is the reason for which IMPATT devices are packaged with heat sinks so that heat can be conducted away from the device during steady state operation. Heat sink dimensions are chosen properly such that total thermal resistance attains such a value that can keep the junction temperature of the device well below the burn-out temperature (different for different base materials) during CW steady state operation of the oscillator.

Schematic diagram of a resonant cap cavity IMPATT oscillator is shown in Figure 1. Heat sink is attached below the device. At the upper side of the device a bias post Figure 1 is connected with the device through package cap and one or more gold plate lead(s) as shown in Figure 2 to supply DC bias current. So if we consider the junction of the device as the heat source during steady state operation of the oscillator then it is clearly visible that there are two paths for heat from the junction to flow towards the ambient. First one is below the junction, i.e. junction → diode portion below the junction → heat sink → ambient. And the second path is above the junction, i.e. junction → diode portion above the junction → gold plat lead(s) → package cap → disc cap & bias post → ambient. Cut way of packaged IMPATT diode is shown in Figure 2.

In this figure the detail structure of the device with the package and heat sink is clearly visible.

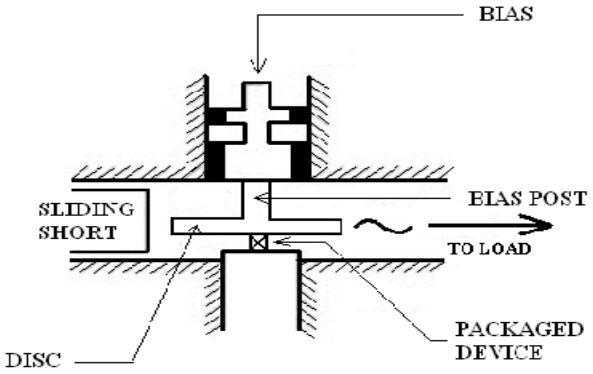

Figure 1. Schematic diagram of W-Band resonant cap cavity

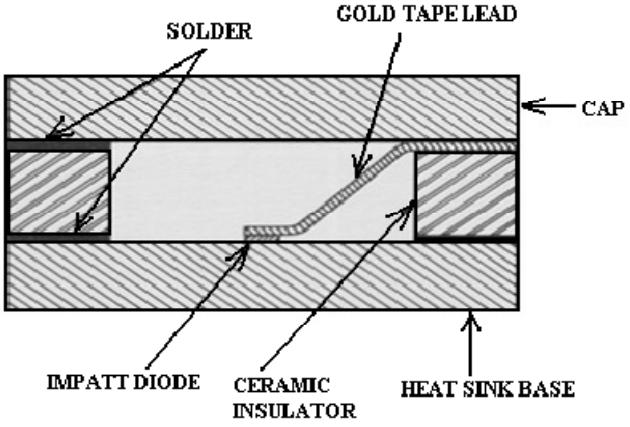

Figure 2. Cut way of Packaged IMPATT Diode

The rest of this paper is organized as follows. Section 2 describes the details of the actual formulation of the Total Thermal Resistance. Section 3 provides the algorithm used to design the heat sinks for IMPATT oscillators to operate in a particular junction temperature during continuous wave steady state operation. Designed Heat Sink Dimensions (using Diamond and Copper both), calculated Total Thermal Resistances and Junction Temperatures for different CW DDR IMPATT diodes with different base materials operating at 94 GHz (W-Band) are studied and compared in Section 4. Results are provided in this section in terms of necessary plots and tables.

2. FORMULATION OF TOTAL THERMAL RESISTANCE

Consider a cylindrical block of a material of face area *A*, thickness *L* and the temperature of the upper and lower faces are T_1 and T_2 *K* respectively ($T_1 > T_2$). So heat will conduct from the hotter face to the colder face. If *Q* be the amount of heat conducted in time *t* second, then it is found that,

$$Q \infty A, T_1 - T_2, t, \frac{1}{L}.$$

$$\Rightarrow Q = \frac{kA(T_1 - T_2)t}{L} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots(1)$$

Where, *k* is a constant, called *thermal conductivity*.

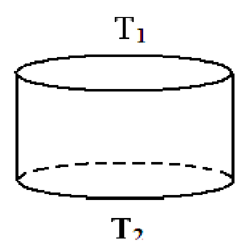

Figure 3. Cylindrical Block

Now the Thermal Resistance can be defined as,

$$R_{th} = \frac{\text{Temperature Change}}{\text{Heat Flow Rate}} = \frac{T_1 - T_2}{\left(\frac{Q}{t}\right)} \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots(2)$$

So, the thermal impedance is defined as the temperature rise produced at the junction by the dissipation of one watt of power. Now, using (1) and (2) the thermal resistance of a cylindrical block can be formulated as,

$R_{th} = \left(\frac{L}{A.k}\right)$, where $A = \pi r^2$ [Cylinder having circular cross section of radius r]................ (3)

In this paper, our aim is to formulate the Total Thermal Resistance of the packaged IMPATT diode over semi-infinite copper/diamond heat sink. In Figure 4 the actual structure of typical Silicon based Ordinary Mesa diode over diamond/copper heat sink is shown. The position of the junction along with different layers of the DDR IMPATT diode is shown in this figure in detail.
To determine the thermal resistance of the mesa diode, for simplicity its actual structure must be approximated properly without losing accuracy significantly. Three steps of approximation of the different layers of the mesa diode are elaborated in the Figure 5.

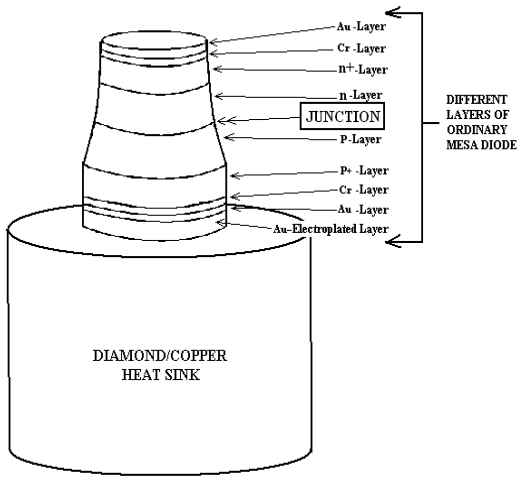

Figure 4. Actual Structures of typical Si based Ordinary Mesa diode over Semi-Infinite Diamond/Copper Heat Sink

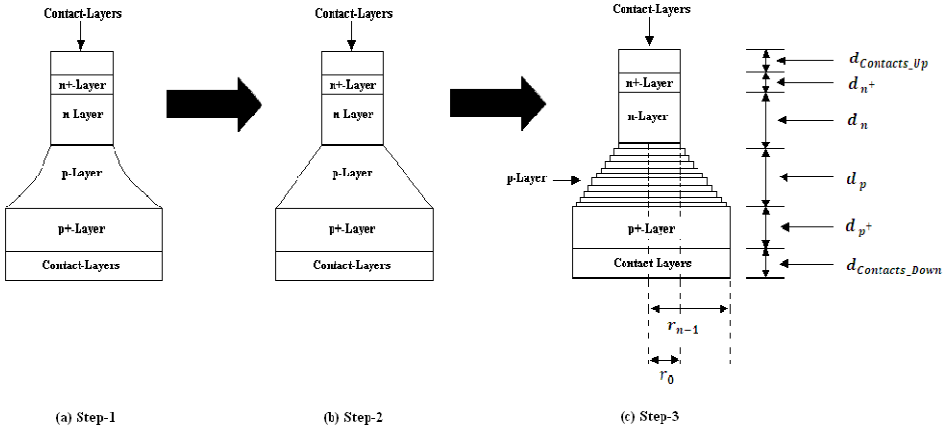

Figure 5. Three Step Approximations for different layers of Ordinary Mesa Structure of DDR IMPATT diode.

In the first step (step-1), different layers are assumed to have the shape described in Figure 5(a). *p*-layer of the mesa DDR diode can be closely approximated to have conical shape (step-2) as shown in Figure 5(b). In the next step (step-3) the *p*-layer of the diode is approximated as *n* number of concentric cylinders having same axial length (*dp/n*) but increasing radius uniformly from r_0 to r_{n-1} (Figure 5(c)). As number of such cylinders (*n*) increases, the approximation comes closer to the conical shape. When $n \rightarrow \infty$, then this approximation (step-3) becomes perfectly conical approximation (step-2) of *p*-layer. Finally *p*+ and contact-layers below the junction together are approximated as a cylinder of fixed radius having the radius r_{n-1}. Generally *p*+ and contact-layers below the junction have square cross-sections, but in our analysis [for simplicity] these cross-sections are approximated as circular. Heat sinks are also assumed as having circular cross sections. Secondly for the portion of the diode above the junction Silicon *n*, *n*+ and contact layers above the *n*+-layer together are approximated as a cylinder of fixed radius having the radius r_0.

Following the above mentioned assumptions for the diode, now the Total Thermal resistance of the ordinary mesa diode along with the heat sink and other package components and bias-post and disc cap will be formulated in this section. A lumped analytical model of heat transfer in ordinary mesa structure of DDR IMPATT diode on semi-infinite heat sink is shown in Figure 6.Here the p-n junction is considered as the constant heat source (Continuous Wave operation).From the junction of the diode the heat will continuously flow upward [through Diode (above the junction portion), Gold Tape Lead(s), Package Cap, Disc cap & Bias-Post] and downward[through Diode (below the junction portion), Heat Sink] to the ambient during the steady state of operation.

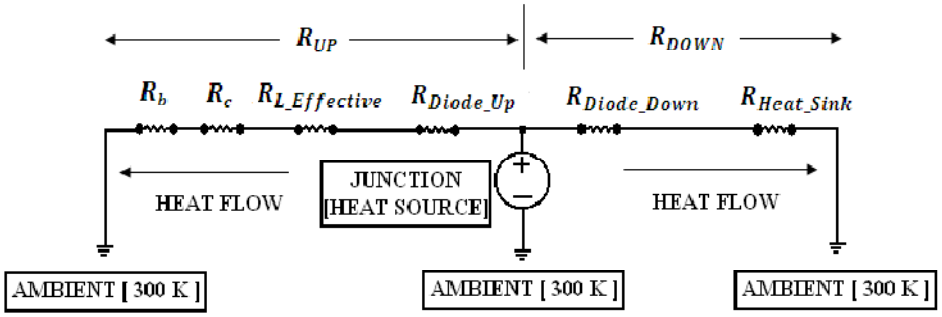

Figure 6. Lumped Analytical Model of Heat Transfer in Ordinary Mesa Structure of DDR IMPATT Diode on Semi-infinite Heat Sink

First consider the downward portion of the heat flow; the thermal resistance associated with that portion. The thermal resistance of the *p*-layer of the diode can be formulated as follows,

$$R_p=\frac{1}{\pi}\underset{n\to\infty}{Lt}\sum_{i=0}^{n-1}\left[\frac{\left(\frac{d_p}{n}\right)}{r_i^2 k_{Base\_Material}}\right] \quad \text{.....(4)}$$

Where, $(r_{i+1}-r_i)=\frac{(r_{n-1}-r_0)}{(n-1)}$ Now the expressions of thermal resistances for p^+ layer is,

$$R_{p^+}=\left[\frac{d_{p^+}}{\pi r_{n-1}^2 k_{Base\_Material}}\right] \quad \text{.....(5)}$$

Combined thermal resistance of the contact-layers below the p+-layer is,

$$R_{Contact\_Down}=\frac{1}{\pi}\sum_{i=0}^{m-1}\frac{d_i}{r_{n-1}k_i} \quad \text{.....(6)}$$

Where, d_i and k_i are the thickness and thermal conductivity of the i^{th} contact layer [assuming total m numbers of contact-layers are present]. Therefore the Total Thermal Resistance of the diode below the junction can be written as,

$$R_{Diode\_Down}=R_p+R_{p^+}+R_{Contact\_Down} \quad \text{.....(7)}$$

Thermal resistance of the Heat Sink will be,

$$R_{Heat\_Sink}= \left[\frac{L_H}{\pi R_H^2 k_H}\right] \text{.....(8)}$$

Where, L_H and R_H are the heat sink thickness and radius respectively. So the Total Thermal Resistance below the junction (Diode + Heat Sink) can be expressed as,

$$R_{Down}= R_{Diode\_Down}+R_{Heat\_Sink} \text{.....(9)}$$

Now the Thermal Resistance of the diode above the junction has to be formulated. Following the assumptions in Figure 5 expressions for Thermal Resistances of the n, n+, and Contact-layers are given below.

$$R_{n\&n^+}= \frac{1}{\pi}\left[\frac{d_n + d_{n^+}}{r_0^2\, k_{Base\_Material}}\right] \text{.....(10)}$$

Where, d_n and d_{n^+} are the thicknesses of the n and n+-layers respectively. Now the combined thermal resistance of the contact-layers over n^+ layer is,

$$R_{Contact\_Up}= \frac{1}{\pi}\sum_{i=0}^{s-1}\frac{d_i}{r_0 k_i} \text{.....(11)}$$

Where, d_i and k_i are the thickness and thermal conductivity of the i^{th} contact layer [assuming total s numbers of contact-layers are present]. Therefore the Total Thermal Resistance of the diode above the junction can be written as,

$$R_{Diode\_Up}= R_{n\&n^+} + R_{Contact\_Up} \text{.....(12)}$$

The expressions of Thermal resistances of Gold Tape Lead(s), Package Cap and Disc Cap and Bias-post are given in (13), (14) and (15) respectively,

$$R_{L\_Effective}= \frac{\left(\frac{L_{Lead}}{A_{Effective\_Lead}\, k_{Au}}\right)}{t} \text{.....(13)}$$

Where, *t* = Number of Lead(s); *t = 1* or *2* or *4*.

$$R_c= \left[\frac{L_{package\_cap}}{A_{effective\_package\_cap}\, k_{Au}}\right] \text{.....(14)}$$

$$R_c= \left[\frac{L_{package\_cap}}{A_{effective\_package\_cap}\, k_{Cu}} + \frac{L_{bias\_post}}{A_{effective\_bias\_post}\, k_{Cu}}\right] \text{.....(15)}$$

So the Total Thermal Resistance above the junction (Diode + Gold Tape Lead(s) + Package Cap+ Disc cap & Bias-post) can be expressed as,

$$R_{UP}=R_{Diode\_up}+R_{L\_effective}+R_c+R_b \text{.....(16)}$$

During the steady state heat will flow take place from the junction (source) to the ambient (sink) via two paths. One path is downward the junction and another is upward the junction. Now expressions for the Thermal Resistances for both of these paths are known from equations (1) to (16). From the lumped analytical model of heat transfer in ordinary mesa structure of DDR IMPATT diode it can be concluded that the Equivalent Total Thermal Resistance of the whole system will be the parallel combination of the Thermal Resistances associated with these two paths.

$$R_{TOTAL=} R_{UP} \parallel R_{DOWN} = \left(\frac{R_{UP} R_{DOWN}}{R_{UP} + R_{DOWN}}\right) = \frac{R_{DOWN}}{1+\left(\frac{R_{DOWN}}{R_{UP}}\right)} \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots(17)$$

Now the cross-sectional area of a gold tape lead is very small compared to the effective diode cross-sectional area. That is way the effective thermal resistance of gold tape lead(s) [$R_{L\_Effective}$] is very large. That makes the value of R_{UP} very much greater compared to R_{DOWN} [$R_{UP} >> R_{DOWN}$]. So, Total Thermal Resistance can be written as,

$$R_{TOTAL}=R_{DOWN} \qquad \text{Since} \quad R_{UP} \gg R_{DOWN}, \qquad \left(\frac{R_{DOWN}}{R_{UP}}\right) \rightarrow 0\ldots\ldots\ldots\ldots\ldots(18)$$

3. ALGORITHM USED TO DESIGN THE HEAT SINKS

In Figure 7 the details of the algorithm used to design the heat sinks for IMPATT oscillators is described as a flow chart. The given algorithm has been implemented by developing a computer program using MATLAB software**.** At the first step, different input parameters (Thermal Conductivities, Thicknesses of different layers of the diode, ambient temperature, breakdown voltage, bias current density and efficiency) Figure 7 are taken as input of the computer program. In the second step, the diode Thermal Resistance is found out using equation (5). Heat sink thickness (L_H) and Radius (R_H) are initialized in the third step. Next in the forth step, the Thermal resistance of the heat sink is determined. In fifth step, the Total Thermal Resistance (Diode-Heat sink combined) is determined using equation (17) and then in the sixth step the Junction Temperature is calculated. Now the calculated Junction Temperature is checked whether it stays between *490 K* and *520 K* (seventh step).

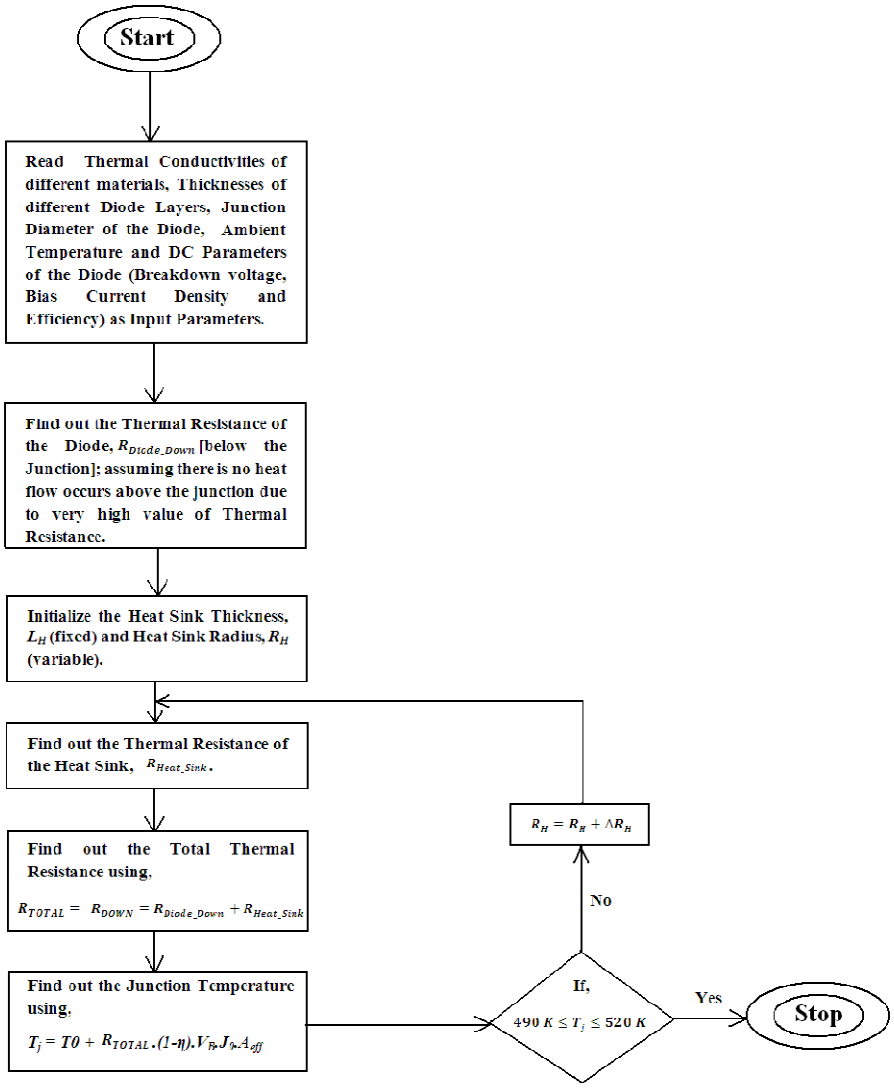

Figure 7. Flow Chart showing the Algorithm for Designing the Heat Sinks.

If yes then the computer program stops and gives the L_H and R_H values as designed values along with corresponding Total Thermal Resistance and Junction Temperature values; if no, then the control goes back to the fourth step with $R_H = R_H + \Delta R_H$ (with a small increment in Heat Sink Radius). In this way the program circulates in that loop until the condition told in seventh step is satisfied.

4. RESULTS AND OBSERVATIONS

The formulated MATLAB program simultaneous solves the required equations and helps in designing CW DDR IMPATT diodes with different base materials and optimized those performances to properly operate at 94 GHz and to study the characteristics of total Thermal resistance versus diode diameter. Structural and simulated DC parameters of those designed diodes are listed in TABLE 1.

TABLE 1: Structural and simulated DC parameters

Base Material & diode structure	Frequency of Operation	*p*-epitaxial layer thickness (μm)	*n*-epitaxial layer thickness (μm)	Bias Current Density (Amp/m^2)	Breakdown Voltage (volt)	Efficiency (%)
Si-DDR	94GHz	0.300	0.400	6.00×10^8	21.98	10.07
4H-SiC-DDR	94GHz	0.555	0.550	1.80×10^8	207.60	16.30

The thicknesses of the all layers of each diode are given in the above table. As we are interested only on the Thermal Resistances of the diodes below the junction so we have used only the thicknesses of *p*+ and contact layers on *p*+ -layer. For Si-DDR, *p*+-layer thickness is taken as *500 nm* and it is coated with a *Cr*-layer about *60 nm* which is followed by an evaporated *Au*-layer of *300 nm*. In case of 4H-SiC-DDR, the thickness of the *p*+ -layer is 900nm and that of the contact layers Ti/Au is 20nm/300nm.

Another two important things we have used in our program to determine the Thermal Resistances of the diodes are (1) Diameters of the diode junctions ($2r_0$) and Diameters of the diodes at diode-heat sink interface ($2r_{n-1}$) and (2) Thermal Conductivities (k) of the all layers. For continuous wave (CW) operation normally junction diameter is, $2r_0$ = 35 μm and diameter of the diodes at diode-heat sink interface is, $2r_{n-1}$ = 350 μm. And the thermal conductivities (at 500 K) of all the materials (diode base materials, contact materials and heat sink materials) are given in tabular form in TABLE 2. Also for determining the thermal resistances of p-layers of the diodes value of n is taken as 100, which is a sufficient approximation for this order of dimensions.

Table 2: Thermal Conductivities

MATERIALS	BASE MATERIAL			CONTACT MATERIALS				HEAT SINK MATERIALS	
	Si	InP	4H-SiC	Au	Ti	Cr	Al	Cu	Type-IIA Diamond
THERMAL CONDUCTIVITY [$WATT/m^0C$]	80	68	370	317	21.9	93.7	237	396	1200

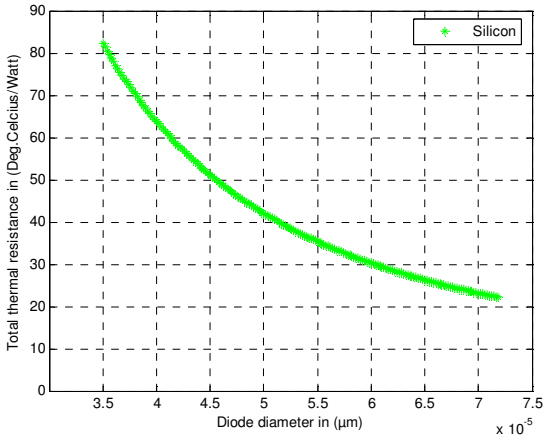

Figure 8. For Silicon based IMPATT DEVICE the graph of the Total thermal resistance of the device as a function of diode diameter with Copper heat sink

Both metallic (copper) and type-IIA diamond are conventionally used as heat sink materials. However a significant thermal advantage is gained by using type-IIA diamond heat sinking. At first to compare the total thermal resistances of all diodes (TABLE 1), heat sink made of copper and diamond of same dimensions (Heat Sink Radius, RH = 175 µm and Thickness, LH = 3000µm) is considered. Taking the values given in table 1 & 2 as inputs in the developed program the total thermal resistances of each diode are plotted as a function of diode diameter (for both copper and diamond of same dimensions).

The graphs obtained are discussed below:

- The graphs obtained from the MATLAB program for Silicon and 4H- SiC IMPATT devices with copper heat sink:
- This graph shows that for 35µm diode diameter of Si-based IMPATT the total thermal resistance is 82.2120 ^{0}c/Watt and with increase of diode diameter the thermal resistance reduces gradually.

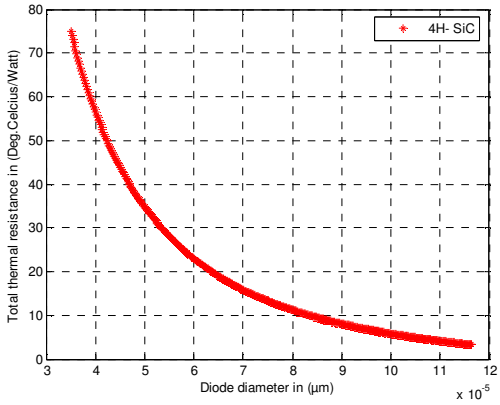

Figure 9.For 4H- Silicon Carbide based IMPATT DEVICE the graph of the Total thermal resistance of the device as a function of diode diameter with Copper heat sink

This graph shows that for 35µm diode diameter of 4H-SiC based IMPATT the total thermal resistance is 74.9286 ^{0}c/Watt and with increase of diode diameter the thermal resistance reduces gradually.

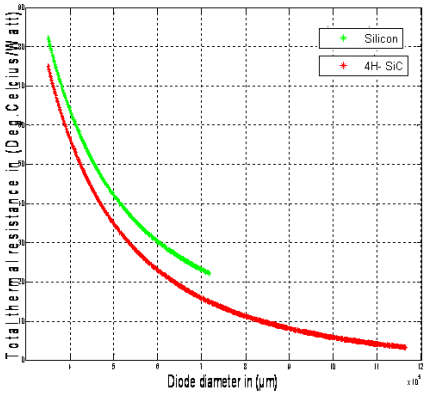

Figure 10.Combinination both the graphs of Silicon based IMPATT device and 4H- Silicon Carbide based IMPATT DEVICE the graph of the Total thermal resistance of the device as a function of diode diameter with Copper heat sink

From figure 10 we can conclude that for our desired diode diameter of 35 µm the Total thermal resistance is very much high for Si-base IMPATT diode with copper heat sink as compared to 4H- SiC based IMPATT diode with copper heat sink. Also we can see that we can increase the diode diameter of 4H- SiC based IMPATT device much more than Si based IMPATT device because the junction temperature reaches between 490K and 520K at higher diode radius in 4H-SiC based IMPATT device than Si based device.

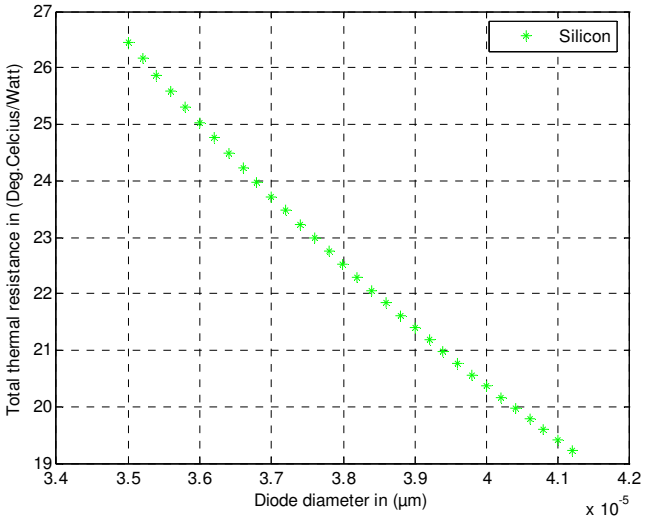

Figure 11. For Silicon based IMPATT DEVICE the graph of the Total thermal resistance of the device as a function of diode diameter with type-IIA diamond heat sink

This graph shows that for 35µm diode diameter of 4H-SiC based IMPATT the total thermal resistance is 26.4556 ^{0}c/Watt and with increase of diode diameter the thermal resistance reduces gradually.

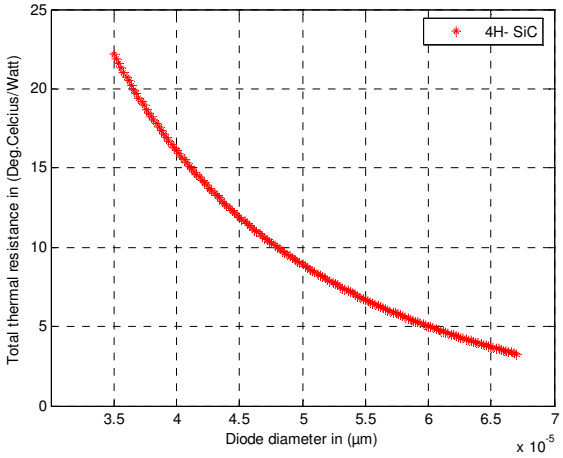

Figure 12. For 4H- Silicon Carbide based IMPATT DEVICE the graph of the Total thermal resistance of the device as a function of diode diameter with type-IIA diamond heat sink.

This graph shows that for 35µm diode diameter of 4H-SiC based IMPATT the total thermal resistance is 22.1722 ^{0}c/Watt and with increase of diode diameter the thermal resistance reduces gradually.

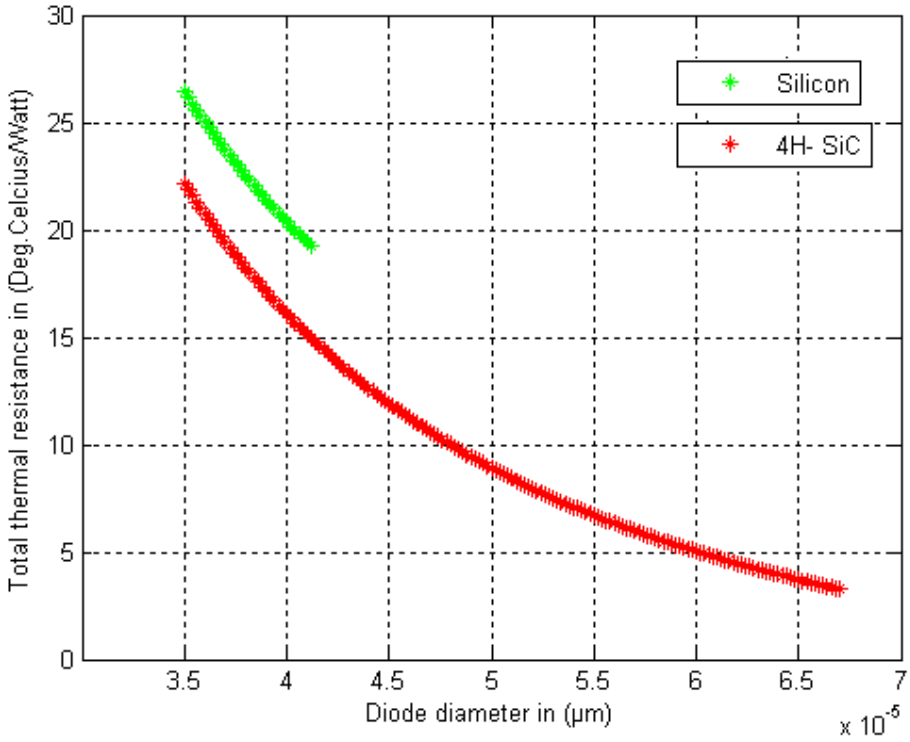

Figure 13.Combination of both the graphs of Silicon based IMPATT device and 4H- Silicon Carbide based IMPATT DEVICE the graph of the Total thermal resistance of the device as a function of diode diameter with type-IIA diamond heat sink

From Figure 13 we can conclude that for our desired diode diameter of 35 μm the Total thermal resistance is very much high for Si-base IMPATT diode with type-IIA diamond heat sink as compared to 4H- SiC based IMPATT diode with type-IIA diamond heat sink. The same observation as was obtained from figure 10. Depending on the thicknesses and thermal conductivities of different layers of the diodes total thermal resistances attained different values for a particular diode diameter.

It is evident from all the six graphs that the total thermal resistance of Si (94 GHz) is larger than 4H-SiC-DDR (94 GHz). These can be explained from TABLE 1. From TABLE 1 it is clear that the dissipated power [$P_{dissipated}$ = (1-η).V_B.J_0.Aeff; where V_B = Breakdown voltage, J_0 = Bias current density, A_{eff}= Effective junction area] is smallest for Si (94 GHz) and largest for 4H-SiC (94 GHz). Eventually, to keep almost same junction temperature [$T_j = T_0 + R_{TOTAL}$. Pdissipated] near 500 K the total thermal resistance [R_{TOTAL}] must be largest for Si (94 GHz) and smallest for 4H-SiC (94 GHz). So, to make R_{TOTAL} largest heat sink radius values [diamond and copper heat sinks] must be smallest [$R_{th} \propto 1/r^2$]; similarly to make R_{TOTAL} smallest heat sink radius values [diamond and copper heat sinks] must be largest. That is way it can be seen that the radius values of both diamond and copper heat sinks are smallest for Si (94 GHz)[smallest heat sink volume] and largest for 4H-SiC (94 GHz) [largest heat sink volume].

The algorithm used here (described in Section 3) only adjusts the heat sink radius values, keeping the heat sink thickness values fixed to obtain the equivalent junction temperature [near *500 K*] during CW steady state operation for a particular diode [for both copper and diamond heat sinks]

5. CONCLUSION

It can concluded from the above discussions and comparisons that for our desired diode diameter of 35 μm we can get high thermal resistance by using Si-based IMPATT diode with either types of heat sinks than 4H-SiC based IMPATT diode with either type of heat sinks. Also we can see that we can increase the diode diameter of 4H- SiC based IMPATT device much more than Si based IMPATT device because the junction temperature reaches between 490K and 520K at higher diode radius in 4H-SiC based IMPATT device than Si based device. By observing the figures 10 & 11 it can also concluded that the diamond heat sink is much smaller in size than copper heat sink for equivalent operation since the thermal conductivity of diamond is almost three times larger than that of copper near *500 K.*

REFERENCES

[1] T. A. Midford, R. L. Bernick, IEEE Trans. on MTT, 1979, vol. MTT-27, no. 5, pp. 483-492.
[2] D. P. Kennedy D, J. Appl. Phys., 1960, vol. 31, p. 1490.
[3] J. Frey, IEEE Trans. Electron Devices, 1972, vol. ED-19, p. 981.
[4] R. L. Bernick, Electronic Letters, 1972, vol. 8, no. 7, p. 180.
[5] J. V. DrLorenzo, W. C. Niehaus, J. R. Velebir, D. E. Iglesias, IEEE Trans. Electron Devices, 1975, vol. ED-22, no. 8, pp. 509-514.
[6] H. S. Carslaw, J. C. Jaeger, Conduction of Heat in Solids, Oxford: Clarendon, 1959.

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